查询NTE5620供应商

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NTE5620
TRIAC
800V_{RM}, 8A, TO220 Full Pack

The NTE5620 TRIAC is designed primarily for full–wave AC control applications, such as light dimmers, heater controls, motor controls, and power supplies; or wherever full wave silicon gate controlled solid state devices are needed. TRIAC type thyristors switch from a blocking to a conducting state for either polarity of applied voltage with positive or negative gate triggering.

Features:

- Blocking Voltage – 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, TO220 Full Pack for Low Thermal Resistance, High Heat Dissipation, and Durability
- Gate Triggering Guaranteed in Four Modes

Absolute Maximum Ratings:

Peak Repetitive Off–State Voltage, V_{DRM}
(T_J = –40° to +125°C, 1/2 Sine Wave 50 to 60H_Z, Gate Open, Note 1) 800V

On–State Current RMS, $I_{T(RMS)}$
(T_C = +80°C, Full Cycle Sine Wave 50 to 60H_Z, Note 2) 8A

Peak Non–Repetitive Surge Current, I_{TSM}
(One Full Cycle, 60Hz, T_C = +125°C, Preceded and followed by rated current) 100A

Peak Gate Power (T_C = +80°C, Pulse Width = 2µs), P_{GM} 16W

Average Gate Power (T_C = +80°C, t = 8.3ms), $P_{G(AV)}$ 350mW

Peak Gate Current (Pulse Width = 2µs), I_{GM} 4A

RMS Isolation Voltage (T_A = +25°C, Relative Humidity ≤ 20%), $V_{(ISO)}$ 1500V

Operating Junction Temperature Range, T_J . . . . . –40° to +125°C

Storage Temperature Range, T_{stg} . . . . . –40° to +150°C

Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 2.2°C/W

Typical Thermal Resistance, Case–to–Sink, R_{thCS} . . . . . 2.2°C/W

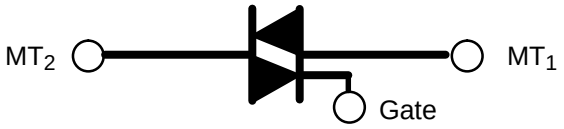
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 60°C/W

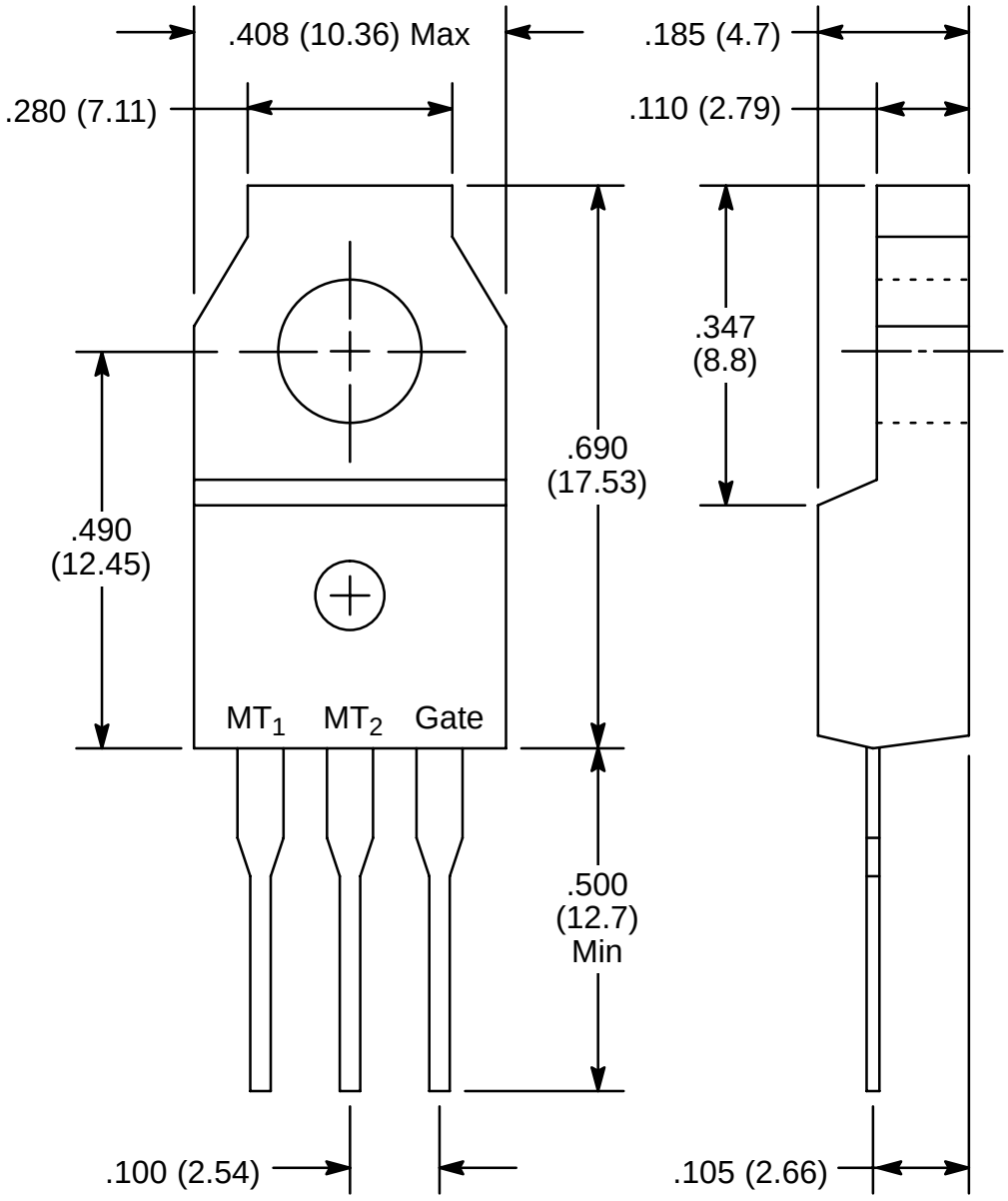
Note 1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

Note 2. The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

Electrical Characteristics: (T_C = +25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) (Rated V_{DRM}, T_J = +125°C, Gate Open)	I_{DRM}	–	–	2	mA
Peak On–State Voltage (Either Direction) (I_{TM} = 11.3A Peak; Pulse Width = 1 to 2ms, Duty Cycle < 2%)	V_{TM}	–	1.7	2.0	V
Peak Gate Trigger Current (Main Terminal Voltage = 12Vdc, R_L = 100 Ohms) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+)	I_{GT}	 – – – –	 – – – –	 50 50 50 75	mA
Peak Gate Trigger Voltage (Main Terminal Voltage = 12Vdc, R_L = 100 Ohms) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–) MT2(–), G(+) (Main Terminal Voltage = Rated V_{DRM}, R_L = 10kΩ, T_J = +125°C) MT2(+), G(+); MT2(+), G(–); MT2(–), G(–) MT2(–), G(+)	V_{GT}	 – – – – 0.2 0.2	 0.9 0.9 1.1 1.4 – –	 2.0 2.0 2.0 2.5 – –	V
Holding Current (Either Direction) (Main Terminal Voltage = 24Vdc, Gate Open I_T = 200mA)	I_H	–	–	50	mA
Critical Rate of Rise of Off–State Voltage (Rated V_{DRM}, Exponential Waveform, T_J = +125°C, Gate Open)	dv/dt	–	100	–	V/µs
Critical Rate of Rise of Commutation Voltage (Rated V_{DRM}, $I_{T(RMS)}$ = 6A, Commutating di/dt = 4.3A/ms, Gate Unenergized, T_C = +80°C)	dv/dt(c)	–	5	–	V/µs


MT2
MT1
Gate


.408 (10.36) Max
.185 (4.7)
.280 (7.11)
.110 (2.79)
.347
(8.8)
.690
(17.53)
.490
(12.45)
MT1
MT2
Gate
.500
(12.7)
Min
.100 (2.54)
.105 (2.66)